	Application No.	Applicant(s)	(pm
Notice of Allowability	10/803,928	NAGASE, KAZUYOS	
	Examiner	Art Unit	<u> </u>
	Anion K. Doh	2050	
	Anjan K. Deb	2858	
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT F of the Office or upon petition by the applicant. See 37 CFR 1.31	S (OR REMAINS) CLOSED i 5) or other appropriate comm RIGHTS. This application is	n this application. If not include unication will be mailed in due	ed course. THIS
1. This communication is responsive to <u>11/08/2005</u> .			
2. The allowed claim(s) is/are <u>3-11</u> .			
3. ☑ Acknowledgment is made of a claim for foreign priority (a) ☑ All b) ☐ Some* c) ☐ None of the:		or (f).	
1. 🖂 Certified copies of the priority documents have			
2. Certified copies of the priority documents have	• •		
Copies of the certified copies of the priority d	ocuments have been receive	ed in this national stage applicat	ion from the
International Bureau (PCT Rule 17.2(a)).			
* Certified copies not received:			
Applicant has THREE MONTHS FROM THE "MAILING DATE noted below. Failure to timely comply will result in ABANDON THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	" of this communication to fil MENT of this application.	e a reply complying with the rec	uirements
4. A SUBSTITUTE OATH OR DECLARATION must be subminFORMAL PATENT APPLICATION (PTO-152) which give	mitted. Note the attached EX ves reason(s) why the oath o	AMINER'S AMENDMENT or Nor declaration is deficient.	OTICE OF
5. CORRECTED DRAWINGS (as "replacement sheets") mu	ust be submitted.		
(a) including changes required by the Notice of Draftspe		w (PTO-948) attached	
1) 🔲 hereto or 2) 🔲 to Paper No./Mail Date			
(b) ☐ including changes required by the attached Examine Paper No./Mail Date	r's Amendment / Comment o	or in the Office action of	
Identifying indicia such as the application number (see 37 CFR each sheet. Replacement sheet(s) should be labeled as such in	1.84(c)) should be written on the header according to 37 C	the drawings in the front (not the FR 1.121(d).	back) of
6. DEPOSIT OF and/or INFORMATION about the dep attached Examiner's comment regarding REQUIREMENT			lote the
Attachment(s) 1. ☑ Notice of References Cited (PTO-892)	5. ☐ Notice of I	nformal Patent Application (PT0	D-152)
2. Notice of Draftperson's Patent Drawing Review (PTO-948)) 6. 🗌 Interview S	Summary (PTO-413),	
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB	Paper No	./Mail Date s Amendment/Comment	
Paper No./Mail Date 4. Examiner's Comment Regarding Requirement for Deposit	8. 🛛 Examiner's	s Statement of Reasons for Allo	wance
of Biological Material	9. 🗌 Other	- frjonhidd	_
		Anjan K Deb Primary Examiner Art Unit: 2858	_

DETAILED ACTION

1. This office action is in response to amendment filed 11/08/2005.

Allowable Subject Matter

2. Claims 3-11 are allowed.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

The primary reason for allowance of the claims is the inclusion of functional circuit having one or a plurality of amplification circuits and said amplification circuit includes an output side amplification circuit for carrying out inputting and outputting of a direct-current signal from an output terminal of said sensor circuit through said connection line, and a reverse current checking means is made to check the reverse current in a transistor of said output side amplification circuit at the occurrence of the disconnection of said connection line in combination with remaining claims limitations.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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Saeki (US 5,615,216) discloses circuit disconnection test circuit comprising plurality of transistors (50,51) connected to test control circuit (Fig. 1).

Sprogis (US 4,801,869) discloses disconnection detection circuit comprising plurality of transistors.

Sher (US 6,449,207 B2) discloses disconnection detection circuit for detecting fuse status comprising plurality of transistors (Fig. 2).

Yamaoka (US 6,943,559 B2) discloses disconnection detection circuit for circuit pattern inspection comprising plurality of conductive lines 20 (Fig. 1).

None of the above prior art references disclose the claimed functional circuit having one or more amplification circuits including output side amplification circuit and a reverse current checking means to check the reverse current in a transistor of said output side amplification circuit at the occurrence of the disconnection of said connection line in combination with remaining claims limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Anjan K. Deb whose telephone number is 571-272-2228. If

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attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached at 571-272-2399.

Anjan K. Deb

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Primary Patent Examiner

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1/12/06